AFFILIATED INSTITUTIONS

ANNA UNIVERSITY, CHENNAI

Regulations – 2009

CURRICULAM AND SYLLABI (I SEMESTER)

M.E – EMBEDDED SYSTEMS

SEMESTER I

COURSE CODE	COURSE TITLE	L	T	P	C
THEORY					
MA9311	Applied Mathematics	3	1	0	4
SY9311	Advanced Digital System Design	3	0	0	3
SY9312	Design of Embedded systems	3	0	0	3
SY9313	Advanced Digital Signal Processing	3	1	0	4
SY9314	Microcontroller System Design And Analysis	3	0	0	3
E1	Elective 1	3	0	0	3
PRACTICAL					
SY9316	Embedded System Lab I	0	0	3	2
	TOTAL CREDITS	**18**	**2**	**3**	**22**

LIST OF ELECTIVES

For SEMESTER I (ELECTIVE – I)

COURSE CODE	COURSE TITLE	L	T	P	C
SY9010	Wireless And Mobile Communication	3	0	0	3
ET9273	Cryptography and Network Security	3	0	0	3
ET9262	Embedded Communication In Software Design	3	0	0	3

MA9311 APPLIED MATHEMATICS L T P C
3 1 0 4

UNIT – I LINEAR ALGEBRAIC EQUATION AND EIGEN VALUE PROBLEMS (12)

System of equations- Solution by Gauss Elimination, Gauss-Jordan and LU decomposition method- Jacobi, Gauss-Seidal iteration method- Eigen values of a matrix by Jacobi and Power method.

UNIT - II WAVE EQUATION (12)

Solution of initial and boundary value problems- Characteristics- D'Alembert's Solution - Significance of characteristic curves - Laplace transform solutions for displacement in a long string - a long string under its weight - a bar with prescribed force on one end- free vibrations of a string.

UNIT - III SPECIAL FUNCTIONS (12)

Bessel's equation - Bessel Functions- Legendre's equation - Legendre polynomials - Rodrigue's formula - Recurrence relations- generating functions and orthogonal property for Bessel functions - Legendre polynomials.

UNIT - IV RANDOM VARIABLES (12)

One dimensional Random Variable - Moments and MGF – Binomial, Poisson, Geometrical, Normal Distributions- Two dimensional Random Variables – Marginal and Conditional Distributions – Covariance and Correlation Coefficient - Functions of Two dimensional random variable

UNIT - V QUEUEING THEORY (12)

Single and Multiple server Markovian queueing models - Steady state system size probabilities – Little's formula - Priority queues - M/G/1 queueing system – P.K. formula.

L:45 T:15 TOTAL: 60 PERIODS

REFERENCES:

1. Sankara Rao.K. "Introduction to Partial Differential Equation ", PHI, 1995.
2. Taha. H.A., "Operations Research- An Introduction " 6th Edition, PHI, 1997.
3. Jain M.K. Iyengar, S.R.K. & Jain R.K., "International Methods for Scientific and Engineering Computation", New Age International (P) Ltd, Publlishers 2003.
4. Kanpur J.N. & Saxena. H.C. "Mathematical Statistics", S.Chand & Co.,New Delhi, 2003.
5. Greweal B.S. "Higher Engineering Mathematics", Khanna Publishers, 2005.

SY9311 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

UNIT – I SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.

UNIT – II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT – III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (9)

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT – IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES (9)

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

UNIT – V SYSTEM DESIGN USING VHDL (9)

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modelling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits – VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

TOTAL: 45 PERIODS

REFERENCES:

1. Donald G. Givone "Digital principles and Design" Tata McGraw Hill 2002.
2. John M Yarbrough "Digital Logic appns. and Design" Thomson Learning, 2001
3. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001
4. Charles H. Roth Jr. "Digital System Design using VHDL" Thomson Learning, 1998.
5. Charles H. Roth Jr. "Fundamentals of Logic design" Thomson Learning, 2004.
6. Stephen Brown and Zvonk Vranesic "Fundamentals of Digital Logic with VHDL Deisgn"Tata McGraw Hill, 2002.
7. Navabi.Z. "VHDL Analysis and Modeling of Digital Systems. McGraw International,1998.
8. Parag K Lala, "Digital System design using PLD" BS Publications, 2003
9. Parag K Lala, " Digital Circuit Testing and Testability" Academic Press, 1997.
10. Peter J Ashendem, "The Designers Guide to VHDL" Harcourt India (P) Ltd, 2002
11. Mark Zwolinski, "Digital System Design with VHDL" Pearson Education, 2004
12. Skahill. K, "VHDL for Programmable Logic" Pearson education, 1996.
13. Nelson V.P., Nagale H.T., Carroll B.D., and Irwin J.D., "Digital Logic Circuit Analysis and Design", Prentice Hall International Inc.1995.
14. Dueck R.K., "Digital Design with CPLD applications and VHDL" Thomson Delmer Learning, 2001.

SY9312 **DESIGN OF EMBEDDED SYSTEMS** **L T P C**
3 0 0 3

UNIT- I **9**

Embedded Design life cycle – Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other issues in selection processes.

UNIT- II **9**

Partitioning decision – Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System startup – Hardware manipulation – memory – mapped access – speed and code density.

UNIT- III **9**

Interrupt Service routines – Watch dog timers – Flash memory Basic toolset – Host ased debugging – Remote debugging – ROM emulators – logic Analyzer – Caches – Computer optimisation – Statistical profiling.

UNIT- IV **9**

In circuit emulators – Buller proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

UNIT- V **9**

Testing – Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

TOTAL: 45 PERIODS

REFERENCES:

1. Arnold S. Berger – Embedded System Design CMP books, USA 2002.
2. Sriram Iyer, “Embedded Real time System Programming”
3. ARKIN, R.C., Behaviour-based Robotics, The MIT Press, 1998.

SY9313 **ADVANCED DIGITAL SIGNAL PROCESSING** **L T P C**

[Review of discrete-time signals and systems- DFT and FFT, Z-Transform, Digital Filters is recommended] **3 1 0 4**

UNIT – I DISCRETE RANDOM SIGNAL PROCESSING (9)

Discrete Random Processing – Expectations – Variance – Co-Variance – Scalar Product – Energy of Discrete Signals – Parseval's Theorem – Wiener Khintchine Relation – Power Spectral Density – Periodogram. Autocorrelation – Sum Decomposition Theorem – Spectral Factorization Theorem – Discrete Random Signal Processing by Linear Systems – Simulation of White Noise – Low Pass Filtering of White Noise.

UNIT – II LINEAR ESTIMATION AND PREDICTION (9)

Maximum likelihood criterion – Efficiency of estimator – Least Mean Squared Error Criterion – Wiener Filter – Discrete Wiener Hoff Equations – Recursive estimators – Kalman filter – Linear prediction – Prediction error – Whitenign fliter – Inverse filter – Levinson recursion – Lattice realization and Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT – III ADAPTIVE FILTERS (9)

FIR adaptive filters – Newton's steepest descent method – Adaptive filter based on steepest descent method – Widrow Hoff LMS adaptive algorithm – Adaptive channel equalization – Adaptive echo chancellor – Adaptive noise cancellation – RLS Adaptive filters – Exponentially weighted RLS – Sliding window RLS – Simplified HR LMS adaptive filter.

UNIT – IV MULTIRATE DIGITAL SIGNAL PROCESSING (9)

Mathematical description of change of sampling rate – Interpolation and Decimation – Continuous time model – Direct digital domain approach – Decimation by an integer factor – Interpolation by an integer factor – Single and multistage realization – Poly phase realization – Application to sub band coding – Wavelet transform and filter bank implementation of wavelet expansion of signals.

UNIT – V DIGITAL SIGNAL PROCESSORS (9)

Fundamentals of Fixed – Point DSP Architecture – Fixed Point Representation of Numbers – Arithmetic Computation – Memory Accessing – Pipelining of Instructions – Features of Example Processors – TMS320C25 – DSP16A and DSP 56001 – Floating Point DSPs – Floating-Point Representation of Numbers – TMS320C30 – Comparison of DSPs – Development Tools for DSP Programming – TMS320C30 Evaluation Module.

L:45 T:15 TOTAL :60 PERIODS

REFERENCES:
1. Monson H. Hayes, 'Statistical Digital Signal Processing and Modeling", John Wiley and Sons Inc., New York, 1996.
2. Sopocles J. Orfanidis, "Optimum Signal Processing", McGraw Hill, 1990.
3. John G. Proakis, Dimitirs G. Monolakis, "Digital Signal Processing", Pearson Education, 1995.
4. Sanjit K. Mitra, "Digital Signal Processing – A Computer based approach", Tata McGraw Hill – 1998.
5. Rabiner and Gold, "Theory and Applications of Digital Signal Processing, A Comprehensive, Industrial – Strength DSP reference book"
6. TMS320C5X User's Guide, Texas Instruments, 1995.

SY9314	MICROCONTROLLER SYSTEM DESIGN AND ANALYSIS	L T P C 3 0 0 3

UNIT -I 8051 ARCHITECTURE 9

Basic organization – 8051 CPU structure – Register file – Interrupts – Timers – Port circuits – Instruction set – Timing diagram – Addressing modes – Simple Program and Applications.

UNIT-II 8051 PROGRAMMING 9

Assembly language programming – Arithmetic Instructions – Logical Instructions –Single bit Instructions – Timer Counter Programming – Serial Communication Programming Interrupt Programming – RTOS for 8051 – RTOSLite – FullRTOS –Task creation and run – LCD digital clock/thermometer using FullRTOS

UNIT-III PIC MICROCONTROLLER 9

Architecture – memory organization – addressing modes – instruction set – PIC progrmming in Assembly & C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming, MP-LAB.

UNIT-IV PERIPHERAL OF PIC MICROCONTROLLER 9

Timers – Interrupts, I/O ports- I^2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing –Flash and EEPROM memories.

UNIT-V SYSTEM DESIGN – CASE STUDY 9

Interfacing LCD Display – Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control – Controlling AC appliances –Measurement of frequency - Stand alone Data Acquisition System.

REFERENCES:

1. John B.Peatman, “Design with Micro controllers”, McGraw Hill international Limited, Singapore, 1989.
2. Michael Slater, “Microprocessor based design A comprehensive guide to effective Hardware design” Prentice Hall, New Jersey, 1989.
3. Ayala, Kenneth, “The 8051 Microcontroller” Upper Saddle River, New Jersey Prentice Hall, 2000..
4. Muhammad Ali Mazidi, Janice Gillispie mazidi. “The 8051 Microcontroller and Embedded systems”, Person Education, 2004.
5. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey ‘ PIC Microcontroller and Embedded Systems using Assembly and C for PIC18’, Pearson Education 2008
6. John Iovine, ‘PIC Microcontroller Project Book ’, McGraw Hill 2000
7. Myke Predko, “Programming and customizing the 8051 microcontroller”, Tata McGraw Hill 2001.

SY9316 EMBEDDED SYSTEMS LABORATOY- I L T P C
0 0 3 2

LIST OF EXPERIMENTS

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers
   i) I/O Programming, Timers, Interrupts, Serial port programming
   ii) PWM Generation, Motor Control, ADC/DAC, LCD and RTC Interfacing, Sensor Interfacing
   iii) Both Assembly and C programming
2. Design with 16 bit processors
   I/O programming, Timers, Interrupts, Serial Communication,
3. Study of one type of Real Time Operating Systems (RTOS)
4. Electronic Circuit Design of sequential, combinational digital circuits using CAD Tools
5. Simulation of digital controllers using MATLAB/LabVIEW .

TOTAL :45 PERIODS

SY9010 WIRELESS AND MOBILE COMMUNICATION

L	T	P	C
3	0	0	3

UNIT – I INTRODUCTION (9)

Wireless Transmission-signal propagation-spread spectrum-Satellite Networks - Capacity Allocation-FAMA-DAMA-MAC

UNIT – II MOBILE NETWORKS (9)

Cellular Wireless Networks-GSM-Architecture-Protocols-Connection Establishment - Frequently Allocation-Routing-Handover-Security-GPRA

UNIT - III WIRELESS NETWORKS (9)

Wireless LAN-IEEE 802.11 Standard-Architecture-Services-Ad.Hoc Network - HiperLan-Blue Tooth

UNIT - IV ROUTING (9)

Mobile IP-DHCP- AdHoc Networks-Proactive and Reactive Routing Protocols - Multicast Routing

UNIT – V TRANSPORT AND APPLICATION LAYERS (9)

TCP over Adhoc Networks-WAP-Architecture-WWW Programming Model-WDPWTLS - WTP-WSP-WAE-WTA Architecture-WML-WML scripts.

TOTAL : 45 PERIODS

REFERENCES:

1. Kaveh Pahlavan, Prasanth Krishnamoorthy, " Principles of Wireless Networks' PHI/Pearson Education, 2003
2. Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, " Principles of Mobile computing", Springer, New york, 2003.
3. C.K.Toh, " AdHoc mobile wireless networks", Prentice Hall, Inc, 2002.
4. Charles E. Perkins, " Adhoc Networking", Addison-Wesley, 2001.
5. Jochen Schiller, " Mobile communications", PHI/Pearson Education, Second Edition, 2003.
6. William Stallings, " Wireless communications and Networks", PHI/Pearson Education, 2002.

ET9273 CRYPTOGRAPHY AND NETWORK SECURITY

L	T	P	C
3	0	0	3

UNIT - I SYMMETRIC CIPHERS 9

Overview – classical Encryption Techniques – Block Ciphers and the Data Encryption standard – Introduction to Finite Fields – Advanced Encryption standard – Contemporary Symmetric Ciphers – Confidentiality using Symmetric Encryption.

UNIT - II PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS 9

Introduction to Number Theory – Public-Key Cryptography and RSA – Key Management – Diffie-Hellman Key Exchange – Elliptic Curve Cryptography – Message Authentication and Hash Functions – Hash Algorithms – Digital Signatures and Authentication Protocols.

UNIT – III NETWORK SECURITY PRACTICE 9

Authentication Applications – Kerbors – X.509 Authentication Service – Electronic mail Security – Pretty Good Privacy – S/MIME – IP Security architecture – Authentication Header – Encapsulating Security Payload – Key Management.

UNIT – IV SYSTEM SECURITY 9

Intruders – Intrusion Detection – Password Management – Malicious Software – Firewalls – Firewall Design Principles – Trusted Systems.

UNIT – V WIRELESS SECURITY 9

Introduction to Wireless LAN Security Standards – Wireless LAN Security Factors and Issues.

TOTAL: 45 PERIODS

REFERENCES:

1. William Stallings, “Cryptography And Network Security – Principles and Practices”, Pearson Education, 3rd Edition, 2003.
2. Atul Kahate, “Cryptography and Network Security”, Tata McGraw Hill, 2003.
3. Bruce Schneier, “Applied Cryptography”, John Wiley and Sons Inc, 2001.
4. Stewart S. Miller, “Wi-Fi Security”, McGraw Hill, 2003.
5. Charles B. Pfleeger, Shari Lawrence Pfleeger, “Security In Computing”, 3rd Edition, Pearson Education, 2003.
6. Mai, “Modern Cryptography: Theory and Practice”, First Edition, Pearson Education, 2003.

ET9262 EMBEDDED COMMUNICATION IN SOFTWARE DESIGN

L	T	P	C
3	0	0	3

UNIT - I **9**

OSI Reference Model – Communication Devices – Communication Echo System Design Consideration Host Based Communication – Embedded Communication System – OS Vs RTOS.

UNIT - II **9**

Software Partitioning – Limitation of strict Layering – Tasks & Modules – Modules and Task Decomposition – Layer2 Switch – Layer3 Switch / Routers – Protocol Implementation – Management Types – Debugging Protocols.

UNIT - III **9**

Tables & other Data Structures – Partitioning of Structures and Tables – Implementation – Speeding Up access – Table Resizing – Table access routines – Buffer and Timer Management – Third Party Protocol Libraries.

UNIT - IV **9**

Management Software – Device Management – Management Schemes – Router Management Management of Sub System Architecture – Device to manage configuration – System Start up and configuration.

UNIT - V **9**

Multi Board Communication Software Design – Multi Board Architecture – Single control Card and UNIT Multiple line Card Architecture – Interface for Multi Board software – Failures and Fault – Tolerance in Multi Board Systems – Hardware independent development – Using a COTS Board – Development Environment – Test Tools.

L :45 TOTAL : 45 PERIODS

REFERENCES:

1. Sridhar .T, “Designing Embedded Communication Software” CMP Books, 2003.